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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,717	12/16/2003	Kiyoshi Kato	0756-7230	5660

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,717	KATO, KIYOSHI	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-14,17 and 20-27* is/are rejected.

7)☒ Claim(s) *1-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 of them*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the response filed on June 22, 2005.

Claims 14 and 27 are identical. Correction is required.

The specification is objected to because "activating layer" (throughout the specification) should read "active layer".

Claims 1-27 are objected to because "activating layer" (at least two occurrences in each of independent claims 1-6 and 17-19) should read "active layer". Claims 13 and 26 are further objected to because "involatile" should read "nonvolatile".

Claims 17, 21, 22 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent Application Publication 2002/0179964 to Kato et al. (Kato), cited in the Information Disclosure Statement filed on August 30, 2004.

With respect to independent claim 17, Kato discloses a semiconductor memory element (see the entire reference, including the Fig. 1C disclosure) comprising a semiconductor [active] layer 105 comprising a channel region 102 and one conductive type impurity region 103 (or 104), a first gate insulating film 106, a charge accumulating layer 107, a second gate insulating film 108, and a control gate electrode 109, wherein the semiconductor memory element is formed over a substrate 101 having an insulating surface; wherein the semiconductor [active] layer includes a metal element (see paragraphs [0059-0061]; wherein the channel region is a crystallized polycrystal semiconductor film (see paragraphs [0057-0059]); and wherein a grain boundary of a crystal grain in the polycrystal semiconductor film is flat or formed with a recessed portion.

Claim 17 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

With respect to dependent claim 21, Kato active layer 105 is a crystallized polycrystal semiconductor film subjected to a heating treatment and adding the metal element (see paragraphs [0059-0061]).

Claim 21 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

With respect to dependent claim 22, Kato's metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au (see paragraph [0061]).

Claim 22 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

With respect to dependent claim 24, Kato further discloses a memory cell array in the shape of a matrix (see paragraph [0088]).

Claim 24 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

With respect to dependent claim 25, Kato's further discloses a ceramic substrate (see paragraph [0058]).

Claim 25 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

With respect to dependent claim 26, Kato further discloses a nonvolatile memory (see the Fig. 7 disclosure, for example).

Claim 26 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Kato.

Claims 1, 8, 9, 11-14 and 27 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over United States Patent Application Publication 2002/0179964 to Kato et al. (Kato), cited in the Information Disclosure Statement filed on August 30, 2004. Note MPEP §2113.

With respect to independent claim 1, Kato discloses a semiconductor memory element (see the entire reference, including the Fig. 1C disclosure) comprising a semiconductor [active] layer 105 comprising a channel region 102 and one conductive type impurity region 103 (or 104), a first gate insulating film 106, a charge accumulating layer 107, a second gate insulating film 108, and a control gate electrode 109, wherein the semiconductor memory element is formed over a substrate 101 having an insulating surface; wherein the semiconductor [active] layer includes a metal element (see paragraphs [0059-0061]; wherein the channel region is a polycrystal semiconductor film (see paragraphs [0057-0059]); and wherein a grain boundary of a crystal grain in the polycrystal semiconductor film is flat or formed with a recessed portion.

Thus although claim 1's semiconductor memory device is formed by a different process than Kato (claim 1 recites that the polycrystal semiconductor film is "crystallized by being continuously scanned at least in the same channel region in irradiating a laser beam"), claim 1's semiconductor memory device appears to be the same as or similar to Kato's semiconductor memory device (note Kato's paragraphs [0058-0059]).

Accordingly, as per MPEP §2113, claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kato.

With respect to dependent claim 8, Kato active layer 105 is a polycrystal semiconductor film subjected to a heating treatment and adding the metal element (see paragraphs [0059-0061]).

Claim 8 is thus rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kato.

With respect to dependent claim 9, Kato's metal element is one kind or a plurality of kinds selected from the group consisting of Fe, Ni, Co, Ge, Sn, Pd, Pt, Cu, and Au (see paragraph [0061]).

Claim 9 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Kato.

With respect to dependent claim 11, Kato further discloses a memory cell array in the shape of a matrix (see paragraph [0088]).

Claim 11 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Kato.

With respect to dependent claim 12, Kato's further discloses a ceramic substrate (see paragraph [0058]).

Claim 12 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Kato.

With respect to dependent claim 13, Kato further discloses a nonvolatile memory (see the Fig. 7 disclosure, for example).

Claim 13 is thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Kato.

With respect to dependent claims 14 and 27, Kato discloses a semiconductor memory device selected from a game machine, a video camera, a head attaching type display, a DVD player, a personal computer, a portable telephone, and a car audio (see paragraph [0124]).

Claims 14 and 27 are thus rejected under 35 U.S.C. §102(b) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Kato.

Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication 2002/0179964 to Kato et al. (Kato), cited in the Information Disclosure Statement filed on August 30, 2004, together with United States Patent 5,643,826 to Ohtani et al. (Ohtani), cited in the Information Disclosure Statement filed on December 16, 2003.

Claims 7 and 20 depend on independent claims 1 and 17, respectively, which are rejected under 35 U.S.C. 102 and/or 35 U.S.C. 103 in view of Kato (see above). Those rejections are incorporated by reference into this rejection of claims 7 and 20.

The difference, therefore, between claims 7 and 20, and Kato is claims 7 and 20 recite that the metal element's concentration falls in the range of $1 \times 10^{16}/cm^3$ through $5 \times 10^{18}/cm^3$.

Ohtani teaches providing a metal element crystallization catalyst with a concentration in the range of $1 \times 10^{16}/cm^3$ through $5 \times 10^{18}/cm^3$ (see the entire patent, including the paragraph bridging columns 8 and 9).

It would have been obvious to one skilled in this art to provide Kato's metal element crystallization catalyst with a concentration in the range of $1 \times 10^{16}/cm^3$ through $5 \times 10^{18}/cm^3$ because Ohtani teaches providing metal element crystallization catalysts with that concentration.

Claims 7 and 20 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Kato together with Ohtani.

Claims 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication 2002/0179964 to Kato et al. (Kato), cited in the Information Disclosure Statement filed on August 30, 2004, together with United States Patent 5,289,027 to Terrill et al. (Terrill).

Claims 10 and 23 depend on independent claims 1 and 17, respectively, which are rejected under 35 U.S.C. 102 and/or 35 U.S.C. 103 in view of Kato (see above). Those rejections are incorporated by reference into this rejection of claims 10 and 23.

The difference, therefore, between claims 10 and 23, and Kato is claims 10 and 23 recite that the memory element's channel length is 0.01 micron through 2 microns.

Terrill teaches that thin film transistors conventionally have a submicron channel length (see the entire patent, including column 1, lines 35-37, for example).

It would have been obvious to one skilled in this art to provide Kato's transistor with a channel length of 0.01 micron through 2.0 microns because Terrill teaches that transistors conventionally have submicron channel lengths.

Claims 10 and 23 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Kato together with Terrill.

Claims 2-6, 18 and 19 would apparently be allowable over the prior art of record if amended to overcome the above objection (to "activating layer").

United States Patent Application Publication 2005/0036382 is related to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner